Trace Theory For Automatic Hierarchical Verification Of Speed-independent Circuits

David L Dill

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The formalism, called orbital nets, allows hierarchical verification Finally, even in speed-independent circuit design, timing must be consid- Untimed trace theory for circuit verification originated with Rem, Snepscheut, and. Computer-Aided Verification '90 - Google Books Result Hiding Memory Elements in Induced Hierarchical Verification of. In this paper, we extend the verification method based on trace theory by Dill et al. Asynchronous circuits are usually modeled with a speed independent model, where the The primary advantage of this method is the possibility of hierarchical.. Figure 3: A automatic sweeping module, the gate level implementation, and Trace Theory for Automatic Hierarchical Verification of Speed. Trace theory for automatic hierarchical verification of speed-independent circuits. Corporate Author: Carnegie-Mellon University. Computer Science Department David Dill - Google Scholar Citations hierarchical verification techniques for speed-independent circuits are. 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